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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,594	07/28/2003	Robert C. Sundahl	884.264US2	4636

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EXAMINER	
NGUYEN, DONGHAI D	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,594	SUNDAHL ET AL.	
	Examiner	Art Unit	
	Donghai D. Nguyen	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 29, 2005 has been entered.

Claim Objections

2. Claim 1 is objected to because of the following informalities: "a second circuit board" (claim 1, line 8) should be: --the second circuit board--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 5-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,818,728 to Rai et al in view of US Patent No. 5,703,394 to Wei et al.

Regarding claim 1, Rai et al disclose a method for manufacturing an interconnected circuit board assembly, the method comprising: fabricating a first circuit board (1) having one or more first bonding pads (2); fabricating a second circuit board (1') having one or more second

bonding pads (2'); placing one or more spacers (4) on one or more first bond pads (2) of the first circuit board (1), wherein the one or more spacers are formed of a conductive material (Cu or Au) that remains in a solid form during attachment of the first circuit board to the second circuit board (Figs. 1); aligning the first circuit board with the second circuit board (1') by engaging the spacers (4) with the openings (See Fig. 1B) in the second circuit board (1') so that one or more second bond pads (2') of the second circuit board align with the one or more first bond pads (Fig. 1C), and the one or more second bond pads make electrical contact with the one or more spacers; and attaching the first circuit board to the second circuit board (Fig. 1C); Rai et al do not teach the second circuit board (1') having multiple optoelectrical display elements which electrically connected to one or more second bonding pads. However, Wei et al teach the circuit board (12) having multiple optoelectrical display elements (11) which electrically connected to one or more bonding pads (16) for forming an organic light emitting device (see Figs. 1-2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Rai by providing the teaching fabricating the circuit board having multiple optoelectrical display elements that electrically connected to one or more bonding pads as taught by Wei et al as to form the organic light emitting device for manufacturing the interconnected circuit board assembly.

Regarding claim 5, see Fig. 1B of Rai et al.

Regarding claims 6-9, Rai et al disclose the step of applying a conductive paste (solder 5) in contact with each of the one or more spacers and heating the conductive (Col. 4, lines 30-36).

Regarding claim 10, Rai et al disclose an insulating material (3, 3' and 8) in an interface region between the first and second circuit.

5. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,891,446 to DiStefano et al in view of Wei et al.

Regarding claims 1 and 4, DiStefano et al disclose a method for manufacturing an interconnected circuit board assembly, the method comprising: fabricating a first circuit board (chip mounting substrate, circuit panel, or circuit board 25 or 102) having one or more first bonding pads (terminals 26 or 126); fabricating a second circuit board (50 or150) having one or more second bonding pads (52 or 152); placing one or more spacers (cores 30 or 134) on one or more first bond pads (26 or126) of the first circuit board (25 or102), wherein the one or more spacers are formed of a conductive material (Cu, Ag, Ni, etc.) that remains in a solid form (Col. 6, lines 40-42) during attachment of the first circuit board to the second circuit board (50 or 150); aligning the first circuit board with the second circuit board (50 or 150) by engaging the spacers (30 or 134) with the openings (See Figs. 1-5) in the second circuit board (50/150)so that one or more second bond pads (52 or 152) of the second circuit board align with the one or more first bond pads (See Figs. 1 and 3), and the one or more second bond pads make electrical contact with the one or more spacers; and attaching the first circuit board to the second circuit board (Figs. 1-5). DiStefano et al do not teach the second circuit board having multiple optoelectrical display elements which electrically connected to one or more second bonding pads. However, Wei et al teach the circuit board (12) having multiple optoelectrical display elements (11) which electrically connected to one or more bonding pads (16) for forming an organic light emitting device (see Figs. 1-2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of DiStefano et al by providing the teaching fabricating the circuit board having multiple optoelectrical display elements that

electrically connected to one or more bonding pads as taught by Wei et al as to form the organic light emitting device for manufacturing the interconnected circuit board assembly.

Regarding claims 2 and 3, DiStefano et al do not teach the forming spacers by electroplating and welding the spacers to the bonding pads. Regarding the limitation as described above it would have been an obvious matter of design choice to form at least one the spacer by electroplating process and further to connect/attach the at least one spacer to the bonding pads by welding, since Applicants have not disclosed that the above forming the spacers by electroplating process and attaching the spacers to the bonding pads by welding is critical and patentable method features that would solve any stated problem or is for any particular purpose and it appears the invention would perform equally well with the teaching as taught by DiStefano et al reference (i.e. see discussion at Col. 11, lines 3-35)

Regarding claims 5-9, DiStefano et al disclose the applying a conductive material (solder 34 or 132 and Col. 11, lines 8-11) in proximity of the spacers (Figs. 1-5) or in contact with each of the one or more spacers and heating the conductive (Col. 7, lines 26-33).

6. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiStefano et al in view of Wei at al as applied above, and further in view of US Patent 5,795,818 to Marrs.

DiStefano/Wei et al as applied and relied above do not disclose the process of injecting an insulated material in an interface region between the first and second circuit boards. Marrs teaches the injecting the insulating material (901,199 and/or 601) into the interface region (Col. 10, lines 47-65) between the first and second circuit boards (201/501) or inserting the insulating material to one of the circuit prior to attaching the first circuit board to the second circuit board

and curing the insulating material (Fig. 7-8) then fully cure the insulating material for protecting the connection from the ambient environment (Col. 10, lines 49-54). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of DiStefano/Wei et al by incorporating the Marrs' teachings as described above in order to facilitate the fabrication process including protecting the connections from the environment.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghai D. Nguyen whose telephone number is (571)-272-4566. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (571)-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DN
December 6, 2005

MINH TRINH
PRIMARY EXAMINER
12/8/05